

IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 1 and 2. These sheets, which include Figs. 1 and 2, replace the original sheets including Figs. 1 and 2.

Attachment: Replacement Sheets

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 18-46 are presently active, Claims 1-17 having been canceled without prejudice, Claims 18-46 having been added by way of the present amendment. No new matter has been added.

In the outstanding Office Action, Figure 1 was objected to for not having a legend such as "Prior Art" and Figure 2 was objected to because the black-boxes have not been provided with text label. Claims 1-17 were objected to because of the informalities. Claims 3, 7, 12 and 16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Maejima et al (U.S. Pat. No. 6,791,392).

Regarding the objection to the drawings, on the replacement sheets, Figure 1 has been labeled with - - Prior Art --, and Figure 2 has been corrected to provide the black-boxes with text label. Thus, it is respectfully submitted that the objection to the drawings has been overcome.

Regarding the objection to the Claims 1-17, Claims 1-17 have been canceled and Claims 18-46 have been added, addressing the informalities. Thus, it is respectfully submitted that the objection to the claims has been overcome.

Regarding the 35 U.S.C. § 112, second paragraph, rejection of Claims 3, 7, 12 and 16, Claims 3, 7, 12 and 16 have been canceled and Claims 18-46 have been added, clarifying the claimed subject matter. Thus, it is respectfully submitted that the 35 U.S.C. § 112, second paragraph, rejection has been overcome.

Regarding the rejection under 35 U.S.C. § 102(e), Applicant respectfully submits that the ground of the rejection has been overcome because, in Applicants' view, newly added

independent Claims 18, 19, 24 and 27 patentably distinguish over the applied references as discussed below.

Claim 18 recites that the gate electrode of the first transistor is configured to be supplied with a first potential of the low voltage power supply. Thus, the invention recited in Claim 18, without additional current consumption while the potential of the low voltage power supply is the first potential, enables to block the shoot-through current even when the potential of a low voltage power supply is switched from the first potential to the reference potential.

On the other hand, Fig.3 of Maejima et al discloses a supply voltage detection circuit (DT), which constitutes a breaking circuit for blocking through currents flowing in the level shift circuit (LS1) (See column 5, lines 38-54). However, the gate electrode of the NMOS transistor (TN31, TN32) is not configured to be supplied with the supply voltage VDDL, which is provided to generate an input signal of the NMOS transistor (TN1). Instead, the gate electrode of the NMOS transistor (TN31, TN32) is connected to the supply voltage detection circuit (DT), which consists of a PMOS transistor (TP3) and a resistor (R). The supply voltage detection circuit (DT) consumes additional current while the supply voltage VDDL is a high voltage (e.g., 3V) because a current flows through the supply voltage detection circuit (DT) to detect the level of the supply voltage VDDL while the supply voltage VDDL is a high voltage (e.g., 3V). Thus, Maejima et al fails to disclose that the gate electrode of the first transistor is configured to be supplied with a first potential of the low voltage power supply and the invention recited in Claim 18 is not anticipated by Maejima et al.

Claim 24 recites that the gate electrode of the first transistor is configured to be supplied with a first potential of a low voltage power supply. Therefore, substantially same arguments as set forth above apply to the rejection of Claim 24.

Claim 19 recites that the gate electrode of the fifth MOSFET is connected to the low voltage power supply and that the gate electrode of the sixth MOSFET is connected to the low voltage power supply. Thus, the invention recited in Claim 19, without additional substantial current consumption while the potential of the low voltage power supply is the first potential higher than the reference potential, enables to block the shoot-through current even when the potential of the low voltage power supply is switched from the first potential to the reference potential.

On the other hand, as set forth above, Fig.3 of Maejima et al discloses that the gate electrode of the PMOS transistor (TN31) is not connected to the power supply, but is connected to the supply voltage detection circuit (DT), which consists of a PMOS transistor (TP3) and a resistor (R). Thus, Maejima et al fails to disclose that the gate electrodes of the fifth MOSFET and the sixth MOSFET are connected to the low voltage power supply and the invention recited in Claim 19 is not anticipated by Maejima et al.

Claim 27 recites that the gate electrode of the fifth MOSFET is connected to the low voltage power supply and that the gate electrode of the sixth MOSFET is connected to the low voltage power supply. Therefore, substantially same arguments for Claim 19 apply to the rejection of Claim 27.

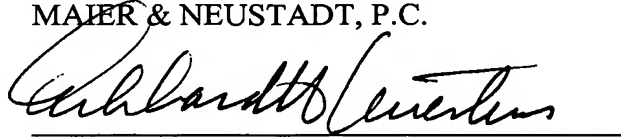
Accordingly, independent Claims 18, 19, 24, and 27 patentably distinguish over Maejima et al. Therefore, independent Claims 18, 19, 24 and 27 and the pending Claims 20-23, 25-26 and 28-46 dependent therefrom are believed to be allowable.

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Reply to Office Action of August 5, 2005

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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